REMARKS/ARGUMENTS

Claim rejections – U.S.C. 102(b)

Claims 1 – 15 were rejected under U.S.C. 102 (b) as being anticipated by Brauch et al.

Response

Claim 1

Brauch et al. claim a method and apparatus for performing a test on a memory in order to determine if said memory has associated defects (col. 2, lines 26-35). The claimed invention similarly performs a test on a memory for determining if the memory has associated defects, but includes the further inventive steps of repeatedly performing the test under different operating environments, then comparing the results for each operating environment to verify the memory integrity. Such stages are not anticipated by Brauch, who only discloses comparing a test result with an expected (i.e. predetermined) result to determine number and location of defects in the memory under test. There is no motivation given by Brauch in the specification for testing **the same** memory under many operating environments, and then comparing test results **with each other** to determine the location and number of memory defects. The extra inventive steps in the claimed invention also give rise to a new result; that is, if the results for each operating environment are the same, i.e. the number and location of defects under each operating condition is the same, then the memory can be deemed to have integrity, **regardless of whether defects are found to exist.** Therefore, applicants assert that the claimed features "testing the memory under the plurality of operating environments, respectively" and "comparing the recorded results for the plurality of operating environments" are neither

taught nor suggested by Brauch's teachings. Reconsideration of claim 1 is respectfully requested.

Claims 2 and 3

Claims 2 and 3 are dependent upon claim 1, and should be allowed if claim 1 is found allowable.

Claims 4 and 5

Under the rejections for claims 4 and 5, the Examiner writes: "when performing any testing memory devices, the voltage supply and temperature of the system must be put into consideration in order to accurately analyzes *(sic)* test data and stabilizes *(sic)* the production lines." This point is only relevant, however, when comparing a memory test result with an expected result, and not when comparing two separate memory test results performed under different operating environments. As clearly illustrated in Brauch Fig. 3, the memory defect searching operation is completed when all memory addresses have been tested under a single operating environment. As voltage supply and temperature must be taken into consideration when comparing a test result with an expected result, **Brauch merely performs the memory test once for a fixed voltage supply condition and/or a fixed temperature condition**. As one can see, Brauch fails to teach or suggest testing the same memory many times in response to different operating conditions corresponding to variance in supply voltage or temperature.

Additionally, claims 4 and 5 are dependent upon claim 1, and should be allowed if claim 1 is found allowable.

Claims 6 and 9

Claims 6 and 9 are dependent upon claim 1, and should be allowed if claim 1 is found allowable.

Claim 7

As stated by the Examiner, Brauch teaches that the accumulated mismatch pairs at the end of the test comprise a complete bitmap of **the precise location of failed cells** in memory that were detected by the particular memory test executed by BIST functional block (col. 3, lines 44-48). However, Brauch does not teach counting the memory defects and then storing the number of memory defects found during the memory test. Therefore, the claimed feature "recording the number of defects detected in the memory" is not anticipated by Brauch's teachings. Additionally, claim 7 is dependent upon claim 1, and should be allowed if claim 1 is found allowable.

Claims 8 and 10

As stated by the Examiner, Brauch teaches obtaining a test result by using a fault locator to perform the comparison between contents read from the memory and the corresponding expected value (col. 3, lines 33-36). However, applicants' disclosure teaches comparing the test results measured under different operating environments to verify the memory integrity. Therefore, the claimed comparing step is neither taught nor suggested by Brauch's teachings.

Additionally, claims 8 and 10 are dependent upon claim 1, and should be allowed if

claim 1 is found allowable.

Claim 11

Referring to the above arguments under Claim 1, applicants assert that the claimed features "testing the memory under a first operating environment", "testing the memory under a second operating environment", and "comparing the first result with the second result" are neither taught nor suggested by Brauch's teachings. Reconsideration of claim 11 is respectfully requested.

Claims 12 and 13

Claims 12 and 13 are dependent upon claim 11, and should be allowed if claim 11 is found allowable.

Claims 14 and 15

Referring to the above arguments under Claims 4 and 5, applicants assert that Brauch fails to teach or suggest testing the same memory many times in response to different operating conditions corresponding to variance in supply voltage or temperature. Additionally, claims 14 and 15 are dependent upon claim 11, and should be allowed if claim 11 is found allowable.

As the limitations of performing tests under different operating environments and

comparing the test results with each other are neither claimed nor anticipated by Brauch et al., applicants believe claims 1 – 15 have been placed in a position for allowance.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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